1 10g 25g High Speed Ethernet Subsystem V2 Xilinx

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1 10g 25g High Speed

10G/25G High Speed Ethernet v2.2 7 PG210 June 7, 2017

www.xilinx.com Chapter 1: Overview Applications IEEE Std 802.3 enables several different Ethernet speeds for Local Area Network (LAN) applications, and 25 Gb/s is the latest addition to the standard. The capability to

(1) 10G/25G High Speed Ethernet Subsystem v2

10G/25G High Speed

Ethernet v2.1 4 PG210 April 5, 2017 www.xilinx.com Product Specification Introduction The Xilinx® 10G/25G High Speed Ethernet subsystem implements the 25G Ethernet Media Access Controller (MAC) wi th a Physical Coding Sublayer (PCS) as specified by the 25G Ethernet Consortium. MAC and physical coding

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10G/25G High Speed Ethernet v1.0 www.xilinx.com 9 PG210 September 30, 2015 Chapter 2: Product Specification Standards The 10G/25G Ethernet core is designed to the standard specified in the 25G and 50G Ethernet Consortium [Ref 1] and the IEEE

Std 802.3 including IEEE 802.3by [Ref 2]. Performance

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10G/25G High Speed Ethernet v2.0 5 PG210 November 30, 2016 www.xilinx.com Chapter 1 Overview This document details the features of the 10G/25G Ethernet Subsystem as defined by the 25G Ethernet Consortium [Ref 1].

PCS functionality is defined by IEEE Standard 802.3, 2015, Clause 49, Physical Coding Sublayer (PCS) for 64B/66B, type 10GBASE-R [Ref 2]. For 25G

(1) 10G/25G High Speed Ethernet Subsystem v2

10G/25G High Speed Ethernet Subsystem implements the 25G Ethernet Media Access Controller (MAC) with a

Physical Coding Sublayer (PCS) as specified by the 25G Ethernet Consortium.

10G/25G High Speed Ethernet Subsystem v3.1 Product Guide

10G/25G High Speed Ethernet v2.4 9 PG210 June 6, 2018 www.xilinx.com Chapter 1:Overview License Type 10G/25G Ethernet PCS/PMA (10G/25G BASE-R) This Xilinx IP module is

provided at no additional cost with the Xilinx® Vivado Design Suite under the terms of the Xilinx End User License. Information about this and other Xilinx IP

10G/25G High Speed Ethernet Subsystem v2

10G/25G High Speed Ethernet v2.3 9 PG210 December 20, 2017 www.xilinx.com Chapter 1: Overview

Standalone 10G/25G Ethernet MAC and PCS/PMA (10G/25G EMAC + 10G/25G BASE-R/KR) or 10G/25G BASE-KR Note: The 10G/25G Ethernet MAC + BASE-R and 10GBASE-KR/25GBASE-KR IP features require separate fee-based licensing.

10G/25G High Speed Ethernet Subsystem v2

10G/25G High Speed

Ethernet v1.2 www.xilinx.com 6 PG210 April 6, 2016 Chapter 1: Overview Optional Features • Clause 73 Auto-Negotiation • Clause 72.6.10 Link Training • Clause 74 FEC - shortened cyclic code (2112, 2080)

10G/25G High Speed Ethernet Subsystem v1

10G/25G High Speed Ethernet Subsystem

implements the 25G Ethernet Media Access Controller (MAC) with a Physical Coding Sublayer (PCS) as specified by the 25G Ethernet Consortium.

10G/25G High Speed Ethernet Subsystem v3.2 Product Guide

10G/25G High Speed Ethernet v1.3 4 PG210 June 8, 2016 www.xilinx.com Product Specification Introduction The

Xilinx® 10G/25G High Speed Ethernet subsystem implements the 25G Ethernet Media Access Controller (MAC) wi th a Physical Coding Sublayer (PCS) as specified by the 25G Ethernet Consortium. MAC and physical coding

10G/25G High Speed Ethernet Subsystem v1

The Xilinx®

LogiCORE™ IP 10G/25G Ethernet solution provides a 10 Gigabit or 25 Gigabit per second (Gbps) Ethernet Media Access Controller integrated with a PCS/PMA in BASE-R/KR modes or a standalone PCS/PMA in BASE-R/KR modes. The core is designed to work with the latest UltraScale™ and UltraScale+™ FPGAs.

10G/25G Ethernet

Subsystem - Xilinx

25G and 100G – optimized high-speed technologies. 25G in the SFP28 form factor: Delivers 2.5 times more performance and bandwidth compared to existing 10G speeds. Supports technology advancements from 10G in packaging and silicon.

Cisco Transceiver Modules - 25GE and 100GE – Enabling ...

• High-performance ARM Cortex-A9 and R5 processors • Flexible I/O configurations of 100M, 1.0G, 2.5G, 5G, 10G, 25G, 40G, and 50G link speeds • Cut-through switching for low-latency applications • Complete TSN feature implementation in industrial temp SKUs including: − Path control and reservation (IEEE 802.1Qca) − Time aware shaper ...

BCM53570 1G/2.5G/10G/25G TSN Connectivity Switch

The Xilinx® 10G/25G High Speed Ethernet subsystem implements the 25G Ethernet Media Access Controller (MAC) with a Physical Coding Sublayer (PCS) as specified by the 25G Ethernet Consortium. MAC and PCS/PMA or PCS/PMA alone are

available. Legacy operation at 10 Gb/s is supported.

10G/25G High Speed Ethernet Subsystem v1

LogiCORE IP 25G/10G High Speed Ethernet Subsystem 25G Media Access Controller with PCS/PMA Project License. Click image to enlarge. Back. Manufacturer: Xilinx. Product Category: Programmable Logic, IP

Cores. Avnet Manufacturer Part #: EF-DI-25G-TSN-802-1-CM-PROJ. Compare. Datasheet.

EF-DI-25G-TSN-802-1-CM-PROJ by Xilinx IP Cores | Avnet

These are taxing the limits of traditional 10G infrastructure. Whether it’s IEEE802.1ax WiFi Access Points or direct wired equipment with copper/fiber ports that

require 1G/2.5G/5G/10G backhaul interfaces, new enterprisenetworks are being built with high speed equipment that now requires 25G ethernet interfaces. Figure 1.

Transforming Enterprise Applications with 25G Ethernet SMF ...

Interoperable with other IEEE-compliant

25G interfaces where applicable Certified and tested on Cisco SFP28 ports for superior performance, quality, and reliability High-speed connectivity compliant to IEEE 802.3by and IEEE 802.3cc. Table 1. Cisco 25G Portfolio

Cisco Transceiver Modules - Cisco 25GBASE SFP28 Modules ...

Hi, I have a ZCU102

with 10G/25G High speed Ethernet Subsystem work well on Linux, with ifconfig, ping, etc .... But when I port that project on ZU9EG custom board based-on ZCU102 hardware, it's not work like on ZCU102. When I probe xilinx_emac.ko When i run ifconfig Link encap is unspec. i don't ...