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6.3 Consider a CMOS ring oscillator consisting of an odd number (n) of identical inverters connected in a ring configuration as shown in Fig. 6. 9. The layout of the ring oscillator is such that the interconnection (wiring) parasitics can be assumed to be zero. Therefore, the delay of each stage is the same, and

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the average gate delay is called the intrinsic delay (P) as long as identical ...

Solved > 6.3 Consider a CMOS ring oscillator consisting of ...

CHAPTER 2 SOLUTIONS 7 1.17 20

transistors, vs. 10 in 1.16(a). 1.18 (c)

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